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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,761	07/26/2001	Jose Sanches	00GR01954248	7474

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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,761	SANCHES ET AL.	
	Examin r	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20,23-26,28-32,34-36,38-41,43-45,47-51,53-55 and 57-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20, 28, 31-32, 38, 41, 47, 50-51 and 57* is/are rejected.

7)☒ Claim(s) *22-26,29,30,34-36,39,40,43-45,48,49,53-55,58 and 59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 20, 23-26, 28-32, 34-36, 38-41, 43-45, 47-51, 53-55, and 57-59 have been examined. Claims 20-24, 28, 31-32, 34-36, 38-41, 43-45,47, 50-51, 53-55, and 57 have been amended as per Applicant's request. Claims 21, 27, 33, 37, 42, 46, 52, and 56 have been cancelled as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as filed on 20 September 2002.

Specification

3. The title of the invention is not descriptive. It is simply a broad description of the field of the invention. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20, 28, 31-32, 38, 41, 47, 50-51 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraboschi et al., U.S. Patent No. 5,930,508 (herein referred to as Faraboschi), in view of Bratt et al., U.S. Patent No. 5,740,402 (herein referred to as Bratt) and in further view of Hennessy and Patterson's "Computer Architecture Quantitative Approach" (herein referred to as Hennessy).

6. Regarding claims 20, 31-32, 41, and 50-51, taking claim 20 as exemplary, Faraboschi has taught a signal processor for executing variable-sized instructions, each instruction comprising up to N codes with N being a positive integer grater than 1 (400 of Fig.4), the signal processor comprising:

a. A program memory (714 of Fig.7) comprising I individually addressable, parallel-connected memory banks with I being a positive integer at least equal to N (see Col.5 line 61 – Col.6 line 7), said program memory comprising a program recorded in an interlaced fashion (see Col.7 lines 49-59),

b. Reading means for reading said program memory by reading a code in each of said I memory banks during a cycle for reading an instruction (see Col.5 line 61 – Col.6 line 7), with each instruction comprising a sequence of codes to be read(see Col.5 line 61 – Col.6 line 7), and when a number of the sequence of codes of the instruction being read is less than I, then codes belonging to a following instruction are read (see Col.5 lines 12-25)

c. Said reading means comprising:

i. Address means for applying to said memory banks individual addresses generated from a collective value of a program counter that is incremented (see Faraboschi, Col.4 lines 29-30), before a beginning of the cycle for reading the instruction, by a value equal to a number of codes comprising a previous instruction (see Faraboschi, Col.2 lines 13-30). Here, while not taught explicitly, it is inherent that a read address be calculated before the

cycle in which the read is performed, as without an address, the read cannot occur.

ii. Filtering means for filtering codes that do not belong to the instruction to be read, using parallelism bits accompanying the codes (see Faraboschi, Col.4 line 57 – Col.5 line 35).

7. Faraboschi has not explicitly taught wherein the program is recorded in the program memory in an interlaced fashion as a function of one code per memory bank and per address applied to said memory banks. Bratt has taught the storing of consecutive instruction codes in consecutive memory banks in an interleaved fashion so that consecutive instruction codes can be read in parallel in a single cycle, thereby increasing the available memory bandwidth and allowing a VLIW processor to service each code in the instruction in parallel, thus increasing access time to the memory without adding more read ports (see Bratt, Col.1 lines 29-64). One of ordinary skill in the art would have recognized that it is desirable to not only increase the speed of a memory access, but to do so without adding additional hardware (read ports) that would otherwise have increased cost. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Faraboschi to store consecutive instruction codes in consecutive memory banks in an interleaved fashion so that the multiple instruction codes could be operated on in parallel, thus increasing the system throughput without adding additional hardware.

8. In addition, Faraboschi in view of Bratt has not taught applying to each of said memory banks an individual read address that is based upon a result of a division by I of the collective value of the program counter. However, Bratt has taught in column 1, lines 31-35 that some

address bits are used to determine which bank and address to address, however, Bratt does not explicitly teach how the address bits are used to determine this. Hennessy has taught interleaved memory banks determine which bank to access by performing a modulo operation on the address and the number of banks (Hennessy page 432). The modulo operation finds the remainder between two numbers, and the remainder is part of the result from a division between two numbers. Please see the attached definitions for more information. A person for ordinary skill in the art at the time the invention was made would have recognized that interleaving memory this way optimizes sequential memory accesses (Hennessy page 432, paragraph 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the interleaved memory scheme of Hennessy in the device of Bratt to optimize sequential memory accesses.

9. Claims 31-32, 41, and 50-51 are nearly identical to claim 20, differing only in claims 31-32 being embodied in a processor, claim 41 in a method for a processor, and claims 50-51 in a method for a signal processor, but all encompassing the same scope as claim 20. Therefore, claims 31-32, 41 and 50-51 are rejected for the same reasons as claim 20.

10. Regarding claims 28, 38, 47 and 57, taking claim 28 as exemplary, Faraboschi in view of Bratt has taught a signal processor according to claim 27, wherein the filtered codes are replaced by no-operation codes (see Faraboschi, Col.7 lines 32-44).

11. Claims 38, 47 and 57 are nearly identical to claim 28, differing only in claim 38 being embodied in a processor, claim 47 in a method for a processor, and claim 57 in a method for a signal processor, but all encompassing the same scope as claim 28. Therefore, claims 38, 47 and 57 are rejected for the same reasons as claim 28.

Allowable Subject Matter

12. Claims 22-26, 29-30, 34-36, 39-40, 43-45, 48-49, 53-55 and 58-59 are allowable over the prior art of record. Further, claims 22-26, 29-30, 34-36, 39-40, 43-45, 48-49, 53-55 and 58-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Please see previous Office Action dated 16 June 2004 for the reasons for allowability.

Response to Arguments

13. Examiner withdraws claim objections regarding claims 20, 23-24, 29, 31, 35-36, 39, 41, 44-45, 48, 50, 54-55 and 58 in favor of the amended claims.

14. Examiner withdraws claim rejections under 35 U.S.C. 112, second paragraph regarding claims 20-59 in favor of the amended claims.

15. Applicant's arguments with respect to claims 20-59 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
13 December 2004

RICHARD L. ELLIS
PRIMARY EXAMINER